

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

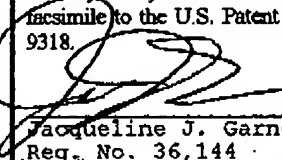
In re the Application of:

Gallia et al.

Serial No.: 10/035,606

Filed: 12/28/2001

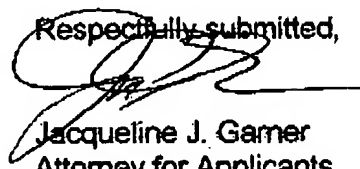
For: METHOD AND SYSTEM FOR REDUCING CHARGE DAMAGE IN SILICON-
ON-INSULATOR TECHNOLOGYDocket No.: TI-32942
Examiner: Hu, S.
Art Unit: 2811
Conf. No.: 3751FAX RECEIVED
JUL 02 2003
TECHNOLOGY CENTER 2800ELECTIONAssistant Commissioner for Patents
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CERTIFICATION OF FACSIMILE TRANSMISSION	
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 Jacqueline J. Garner Reg. No. 36,144	Date 7/2/2003

Dear Sir:

With respect to the Restriction Requirement mailed on 6/12/2003, the Examiner has restricted the instant application to the invention of Group I (Claims 1-11 and 17-20), or Group II (Claims 12-16). In light of this, Applicants elect to pursue Group I, (Claims 1-11 and 17-20) without traverse.

Respectfully submitted,


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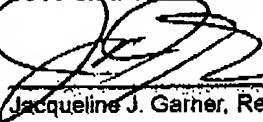
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Jacqueline J. Garner, Reg. No. 38,144

July 2, 2003

Date

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<input type="checkbox"/> CONTINUATION APP'N (# Pages)		<input checked="" type="checkbox"/> Election
<input type="checkbox"/> DIVISIONAL APP'N		
NAME OF INVENTOR(S): Gallia		RECEIPT DATE & SERIAL NO.: Serial No.: 10/035,606
TITLE OF INVENTION: Method and System for Reducing Charge . . .		Filing Date: 12/28/2001
TI FILE NO.: TI-32942	DEPOSIT ACCT. NO.: 20-0668	
FAXED: 7/2/2003		
DUE: 7/12/2003		
ATTY/SECY: JG		

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